



CY7C3385A
CY7C3386A

UltraLogic™ 3.3V High Speed 4K Gate CMOS FPGA

Features

- **Very high speed**
 - Loadable counter frequencies greater than 80 MHz
 - Chip-to-chip operating frequencies up to 60 MHz
- **Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic**
- **High usable density**
 - 16 x 24 array of 384 logic cells provides 12,000 total available gates
 - 4,000 typically usable "gate array" gates in 84-pin PLCC, 100-pin and 144-pin TQFP
- **Low power, high output drive**
 - Standby current typically 250 μ A
 - 16-bit counter operating at 80 MHz consumes 20 mA
- **Flexible logic cell architecture**
 - Wide fan-in (up to 14 input gates)
 - Multiple outputs in each cell
 - Very low cell propagation delay (1.7ns typical)
- **Powerful design tools—Warp3™**
 - Designs entered in IEEE 1164 VHDL, schematics, or both
 - Fast, fully automatic place and route
 - Waveform simulation with back annotated net delays
- PC and workstation platforms
- **Extensive 3rd party tool support**
- **5V tolerant Inputs (see I_{IH} spec)**
- **Robust routing resources**
 - Fully automatic place and route of designs using up to 100 percent of logic resources
 - No hand routing required
- **80 (7C3385A) to 114(7C3386A) bidirectional input/output pins**
- **6 dedicated input/high-drive pins**
- **2 clock/dedicated input pins with fan-out-independent, low-skew nets**
- **Input hysteresis provides high noise immunity**
- **Thorough testability at 3.3V**
 - Built-in scan path permits 100 percent factory testing of logic and I/O cells
- **0.65 μ CMOS process with ViaLink™ programming technology**
 - High-speed metal-to-metal link
 - Non-volatile antifuse technology
- **84-pin PLCC is pinout compatible with 2K (CY7C3384A) devices**
- **100-pin TQFP is pinout compatible with 3.3V 1K (CY7C3382A) and 2K (CY7C3384A) devices**
- **Pinout compatible with 5V 4K (CY7C385P/6P) devices**

Functional Description

The CY7C3385A and CY7C3386A are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 384 logic cell field-programmable gate array (FPGA) offers 4,000 typically usable "gate array" gates. This is equivalent to 12,000 EPLD or LCA gates. The CY7C3385A is available in a 84-pin PLCC and the 100-pin TQFP packages. The CY7C3386A is available in 144-pin TQFP package.

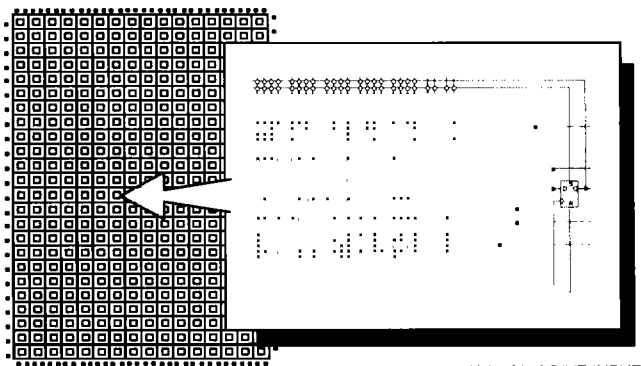
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 80 MHz. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C3385A and CY7C3386A using Cypress Warp3 software or one of several third-party tools. See the tools section of the *Programmable Logic Databook* for more tools information. Warp3 is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C3385A and CY7C3386A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

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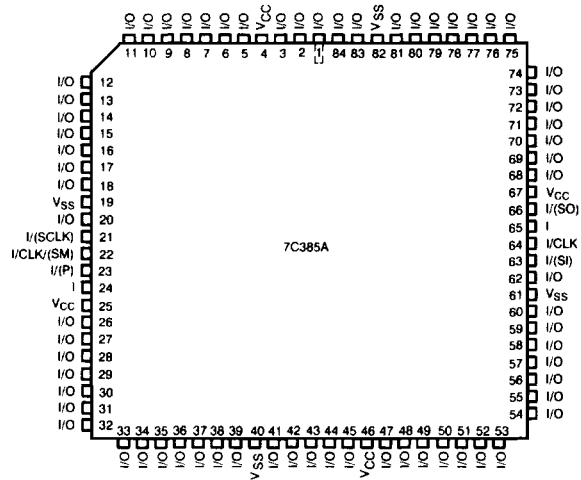
Logic Block Diagram



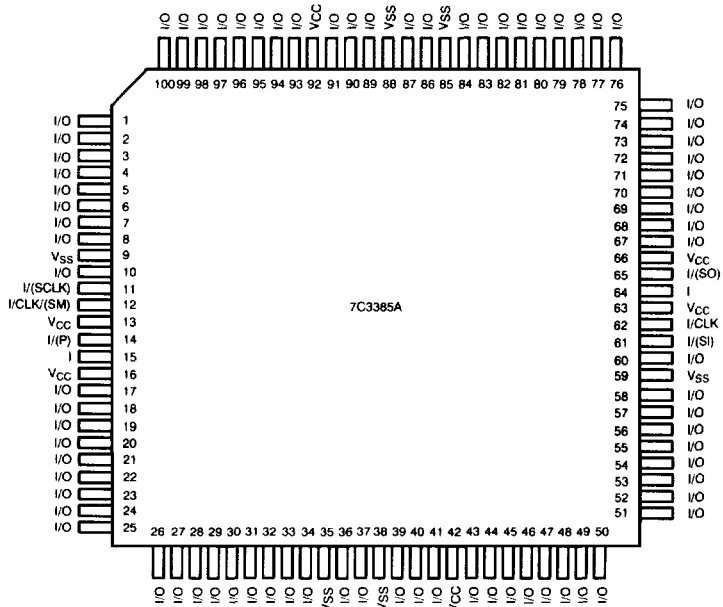
84, 100, and 144 PINS, 114 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

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Pin Configurations (continued)
**PLCC/CLCC
Top View**


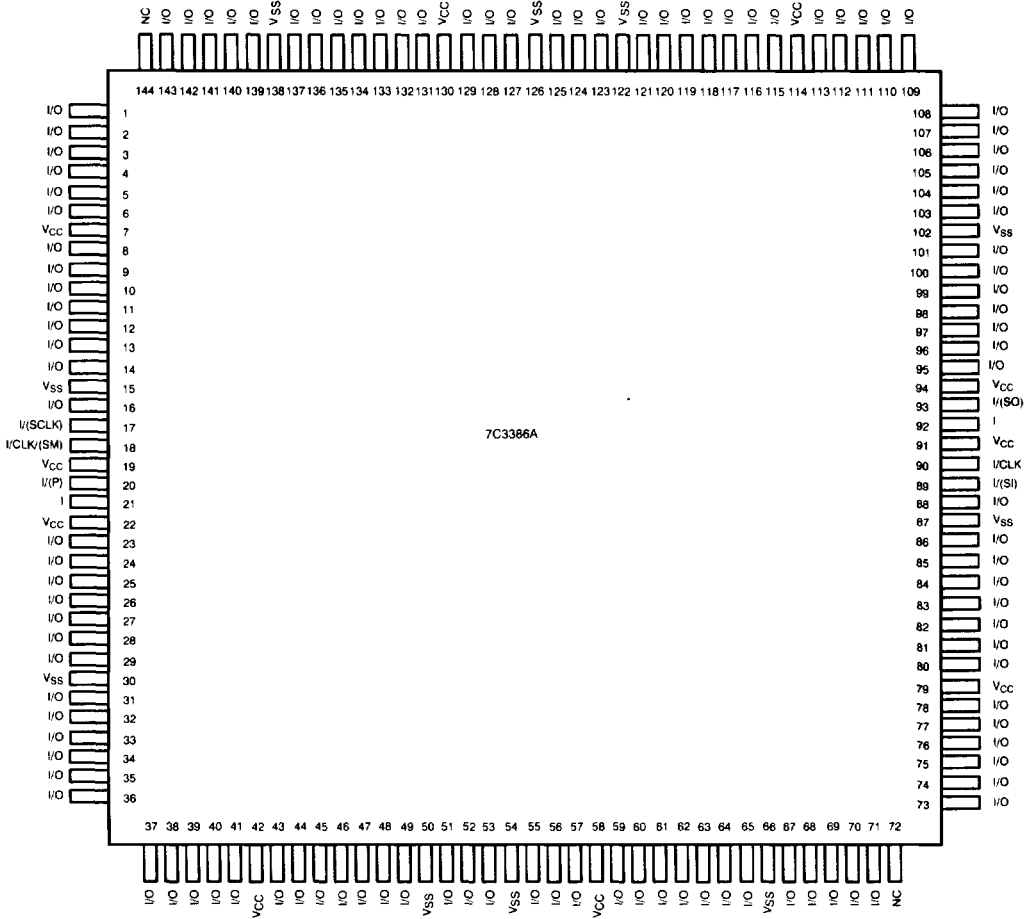
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**TQFP
Top View**


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Pin Configurations (continued)

TOPFP
Top View



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
 Ceramic -65°C to +150°C
 Plastic -40°C to +125°C
 Lead Temperature 300°C
 Supply Voltage -0.5V to 7.0V
 Input Voltage -0.5V to V_{CC} + 0.7V
 ESD Pad Protection ±2000 V
 DC Input Voltage -0.5V to 7.0V

DC Input Current ±20 mA
 Latch-Up Current ±200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3V ± 0.3V
Industrial	-40°C to +85°C	3V ± 0.3V

Delay Factor (K)

Speed Grade	Commercial		Industrial	
	Min.	Max.	Min.	Max.
-X	0.46	3.52	0.40	3.77
-0	0.46	2.61	0.40	2.81
-1	0.46	2.23	0.40	2.39

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = 2.4 mA	2.4		V
		I _{OH} = -10.0 μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage	I _{OL} = 4 mA		0.4	V
		I _{OL} = 10.0 μA		0.1	V
V _{IH}	Input HIGH Voltage		2.0		V
V _{IL}	Input LOW Voltage			0.8	V
I _{IH}	Input HIGH Current Sink (for 5V Inputs)	5V > V _{IN} > V _{CC}		12 ^[1]	mA
I _I	Input Leakage Current	V _{IN} = V _{CC} or V _{SS}	-10	+10	μA
I _{OZ}	Three-State Output Leakage Current	V _{IN} = V _{CC} or V _{SS}	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[2]	V _{OUT} = V _{SS}	-5	-50	mA
		V _{OUT} = V _{CC}	15	100	mA
I _{CC1}	Standby Supply Current	V _{IN} , V _{IO} = V _{CC} or V _{SS}		650	μA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance ^[3]	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3 V	10	pF
C _{OUT}	Output Capacitance		10	pF

Note:

- User must limit input current to 12 mA.
- Only one output at a time. Duration should not exceed 30 seconds.
- C₁ = 45 pF max. on I(SI) and I(P). Capacitance is sample tested.

Switching Characteristics ($V_{CC}=3.3V$, $T_A=25^\circ C$, $K=1.00$)

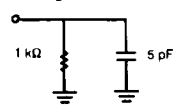
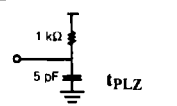
Parameter	Description	Propagation Delays ^[4] with Fanout of					Unit
		1	2	3	4	8	
LOGIC CELLS							
t_{PD}	Combinatorial Delay ^[5]	1.7	2.2	2.6	3.2	5.3	ns
t_{SU}	Set-Up Time ^[5]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.2	2.6	3.2	5.3	ns
t_{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.4	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays ^[4]						Unit
		1	2	3	4	8	12	
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.8	2.9	3.0	3.1	4.0	5.3	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.0	3.1	3.2	3.3	4.1	5.7	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.9	4.7	6.5	ns
t_{GCK}	Clock Buffer Delay ^[6]	2.7	2.8	2.9	3.0	3.1	3.3	ns
t_{GCKHI}	Clock Buffer Min. HIGH ^[6]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKLO}	Clock Buffer Min. LOW ^[6]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays ^[4] with Output Load Capacitance (pF) of					Unit
		30	50	75	100	150	
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTH}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State ^[7]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State ^[7]	3.3					ns

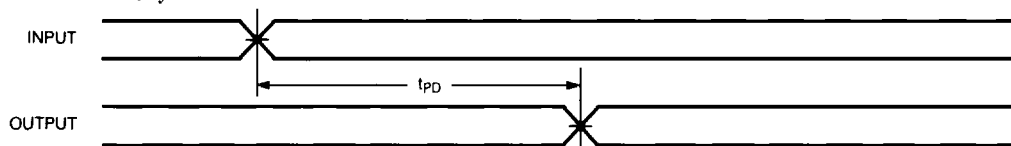
Notes:

- Worst-case propagation delay times over process variation at $V_{CC} = 3.3V$ and $T_A = 25^\circ C$. Multiply by the appropriate delay factor, K , for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
- These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC380 logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
- Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
- The following loads are used for t_{pxz} :

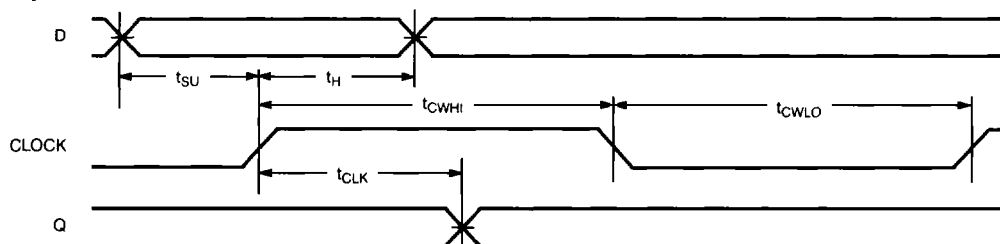



High Drive Buffer K=1.00

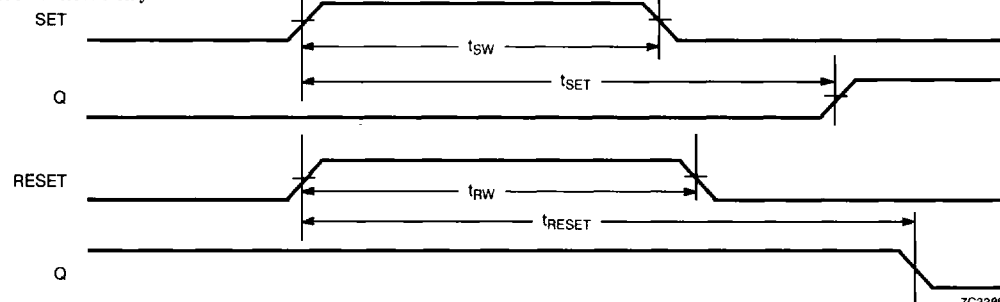
Parameter	Description	# High Drives Wired Together	Propagation Delays ⁽⁴⁾ with Fanout of					Unit
			12	24	48	72	96	
t_{IN}	High Drive Input Delay	1	5.3	6.7				ns
		2		4.5	6.6			ns
		3			5.3	6.2	7.2	ns
		4				5.4	6.2	ns
t_{NI}	High Drive Input, Inverting Delay	1	5.7	7.2				ns
		2		4.6	6.8			ns
		3			5.5	6.4	7.4	ns
		4				5.6	6.4	ns

Switching Waveforms
Combinatorial Delay


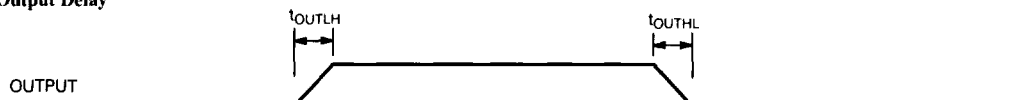
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Set-Up and Hold Times


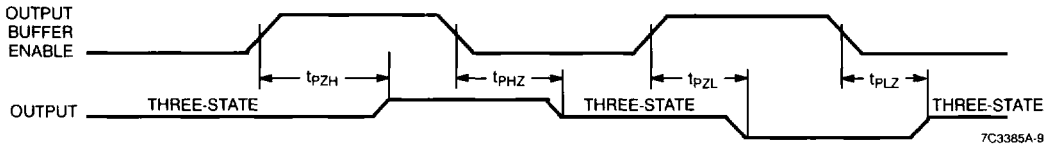
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Set and Reset Delays


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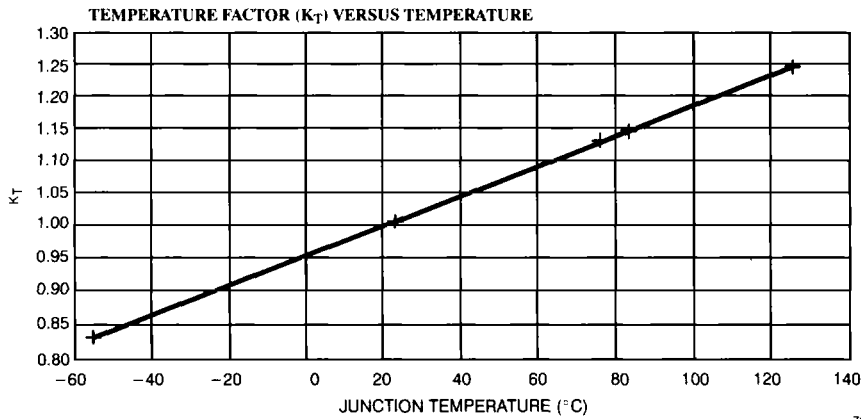
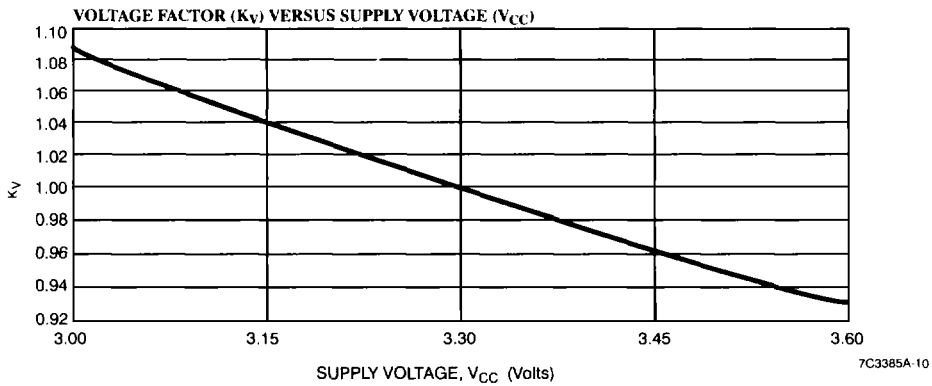
Output Delay


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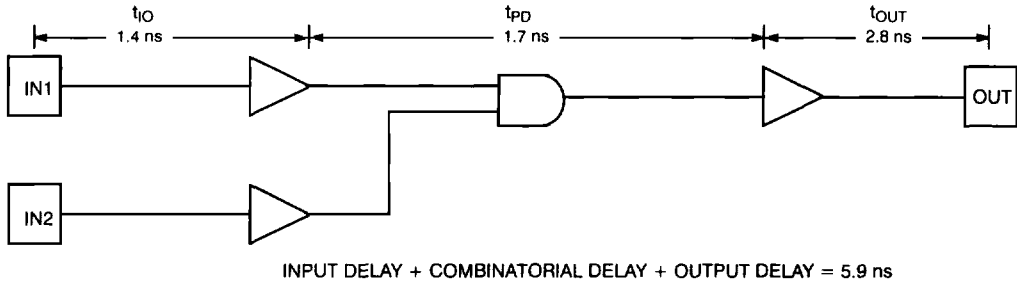
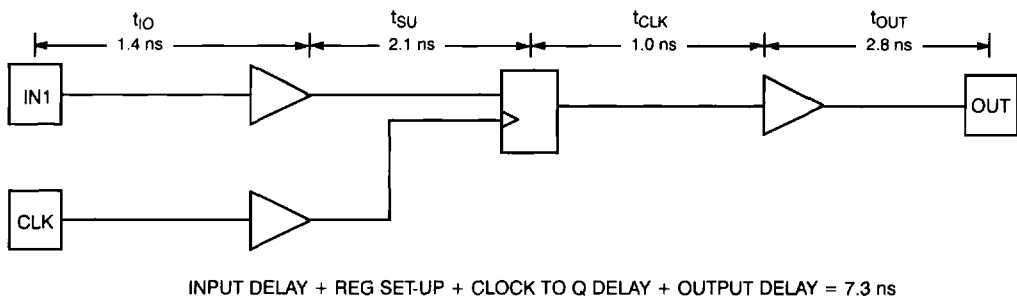
Switching Waveforms (continued)
Three-State Delay

Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate

Delay Factor, K , as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.



* $\theta_{JA} = 45^\circ\text{C/WATT}$ FOR PLCC

Combinatorial Delay Example (Load = 30 pF, K=1, Fanout=1)

Sequential Delay Example (Load = 30 pF, K=1, Fanout=1)




Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
1	CY7C3385A-1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C3385A-1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C3385A-1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C3385A-1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C3385A-0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C3385A-0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C3385A-0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C3385A-0JI	J83	84-Lead Plastic Leaded Chip Carrier	
X	CY7C3385A-XAC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C3385A-XJC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C3385A-XAI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C3385A-XJI	J83	84-Lead Plastic Leaded Chip Carrier	

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
1	CY7C3386A-1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C3386A-1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
0	CY7C3386A-0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C3386A-0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
X	CY7C3386A-XAC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C3386A-XAI	A144	144-Pin Thin Quad Flat Pack	Industrial

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